CLAIMS

1. A method for sensing a programmed/erased state of a selected non-volatile memory (NVM) cell within a memory array, the memory array including a first bit line connected to a first terminal of the selected NVM cell, a second bit line connected to a second terminal of the selected NVM cell, a second NVM cell having a first terminal connected to the second bit line, and a third bit line connected to a second terminal of the second NVM cell, the method comprising:

during a first phase, coupling the first bit line to a first voltage source having a first non-zero voltage level, and coupling the second and third bit lines to a ground source;

during a second phase beginning at an end of the first phase:

decoupling the second bit line from the ground source, whereby a sensed cell signal develops on the second bit in response to a cell current passing through the selected NVM cell from the first bit line, and

decoupling the third bit line from the ground source, and then coupling the third bit line to a current source such that a forced neighbor signal is generated on the third bit line; and

during a third phase subsequent to the second phase and before the sensed cell signal is stabilized, comparing the sensed cell signal generated on the second bit line with a reference signal to determine the programmed/erased state of the selected NVM cell.

2. The method according to Claim 1, wherein a programmed/erased state of the selected NVM cell controls a current through the sensed cell signal during the second and third phases such that a first, relatively small current is

generated on the second bit line when the selected NVM cell is programmed, and a second, relatively large current is generated on the second bit line when the selected NVM cell is erased, and

wherein coupling the third bit line to the current source comprises generating a third current that is between the first and second currents.

3. The method according to Claim 1, wherein coupling the third bit line to the current source comprises generating the forced neighbor signal such that, at a selected time during the third phase, an instantaneous voltage level of the forced neighbor signal is within a range defined by one-half of the reference signal and 1.5 times the reference signal.

4. The method according to Claim 3, wherein coupling the third bit line to the current source comprises generating the forced neighbor signal such that, at the selected time during the third phase, the forced neighbor signal is substantially equal to the reference signal.

5. The method according to Claim 1,

wherein the memory array further comprises a third NVM cell having a first terminal connected to the third bit line and a fourth bit line connected to a second terminal of the third NVM cell, and

wherein the method further comprises:

coupling the fourth bit line to the ground source during the first phase; and

decoupling the fourth bit line from the ground source, and coupling the fourth bit line to the current source during the second and third phases.

6. The method according to Claim 1,

wherein the memory array further comprises a third NVM cell having a first terminal connected to the third bit line and a fourth bit line connected to a second terminal of the third NVM cell, and

wherein the method further comprises:

coupling the fourth bit line to the ground source during the first phase; and decoupling the fourth bit line from the ground source, and coupling the fourth bit line to a second current source during the second and third phases such that a second forced neighbor signal is generated on the fourth bit line, wherein the second forced neighbor signal is substantially equal to the forced neighbor signal generated on the third bit line.

7. A method for sensing a programmed/erased state of a selected non-volatile memory (NVM) cell within a memory array, the memory array including a first bit line connected to a first terminal of the selected NVM cell, a second bit line connected to a second terminal of the selected NVM cell, a second NVM cell having a first terminal connected to the second bit line, and a third bit line connected to a second terminal of the second NVM cell, the method comprising:

during a first phase, coupling the first bit line to a first voltage source having a first non-zero voltage level, and coupling the second and third bit lines to a ground source;

during a second phase beginning at an end of the first phase:

decoupling the second bit line from the ground source, whereby a sensed cell signal develops on the

second bit in response to a cell current passing through the selected NVM cell from the first bit line, and

decoupling the third bit line from the ground source, and coupling the third bit line to a forced neighbor signal such that a voltage level increases on the third bit line from ground to at a predetermined rate; and

during a third phase subsequent to the second phase, and before the voltage level on the third bit line has reached a maximum voltage level, comparing the sensed cell signal generated on the second bit line with a reference signal to determine the programmed/erased state of the selected NVM cell.

8. The method according to Claim 7,

wherein a programmed/erased state of the selected NVM cell controls a current through the sensed cell signal during the second and third phases such that the sensed cell signal increases from ground to the first voltage level at a first, relatively slow rate when the selected NVM cell is programmed, and increases from ground to the first voltage level at a second, relatively fast rate when the selected NVM cell is erased, and

wherein coupling the third bit line to the forced neighbor signal comprises causing the predetermined rate of the voltage level on the third bit line to be between the first and second rates.

9. The method according to Claim 7, wherein coupling the third bit line to the forced neighbor signal comprises generating the voltage level on the third bit line such that, at a selected time during the third phase, the voltage level

is within a range defined by one-half of the reference signal and 1.5 times the reference signal.

10. The method according to Claim 9, wherein coupling the third bit line to the forced neighbor signal comprises generating the voltage level on the third bit line such that, at the selected time during the third phase, the voltage level is substantially equal to the reference voltage.

11. The method according to Claim 7,

wherein the memory array further comprises a third NVM cell having a first terminal connected to the third bit line and a fourth bit line connected to a second terminal of the third NVM cell, and

wherein the method further comprises:

coupling the fourth bit line to the ground source during the first phase; and decoupling the fourth bit line from the ground source, and coupling the fourth bit line to the forced neighbor signal during the second and third phases.

12. The method according to Claim 7,

wherein the memory array further comprises a third NVM cell having a first terminal connected to the third bit line and a fourth bit line connected to a second terminal of the third NVM cell, and

wherein the method further comprises:

coupling the fourth bit line to the ground source during the first phase; and decoupling the fourth bit line from the ground source, and coupling the fourth bit line to a second forced neighbor signal during the second and third phases, wherein the second forced neighbor signal is

substantially equal to the forced neighbor signal generated on the third bit line.

13. A memory circuit comprising:

a memory array including a first non-volatile memory (NVM) cell, a first bit line connected to a first terminal of the first NVM cell, a second bit line connected to a second terminal of the first NVM cell, a second NVM cell having a first terminal connected to the second bit line, and a third bit line connected to a second terminal of the second cell;

a switching circuit connected between each of the first, second and third bit lines and a first voltage source having a first voltage level, a ground source, a sense amplifier, and a secondary signal source; and

means for controlling the switching circuit such that:

during a first phase, the first bit line is coupled to the first voltage source, and the second and third bit lines are coupled to the ground source; and

at the end of the first phase, the second bit line and the third bit line are decoupled from the ground source, the second bit line is coupled to the sense amplifier, the third bit line is coupled to the secondary signal source, and a gate voltage is applied to the gate terminals of the first NVM cell and the second NVM cell, thereby causing a cell current to pass through the first NVM cell and to produce a sensed cell signal on the second bit line that increases from ground to the first voltage level at a development rate determined by the programmed/erased state of the selected NVM cell,

wherein the secondary signal source generates a forced neighbor signal on the third bit line such that a voltage

level on the third bit line increases from ground at a second rate that is similar to the development rate.

14. The memory circuit according to Claim 13, wherein said control means further comprises means for comparing the sensed cell signal generated on the second bit line with a reference signal to determine the programmed/erased state of the selected NVM cell before the forced neighbor signal has reached a maximum voltage level.

15. The memory circuit according to Claim 13,

wherein the switching circuit further comprises a decoder circuit having a first set of terminals connected to each of the first, second and third bit lines, and a second set of terminals including a first terminal connected to the first voltage source via a first signal line, a second terminal connected to the sense amplifier via a sensing line, and a third terminal connected to the current source via a second signal line, and

wherein the first and second signal lines are selectively coupled to ground via a first transistor and a second transistor, respectively.

16. The memory circuit according to Claim 15, wherein the first and second transistors are connected to receive a first control signal such that the first and second transistors are turned on simultaneously.

17. The memory circuit according to Claim 13, further comprising:

a third NVM cell having a first terminal connected to the third bit line and a fourth bit line connected to a second terminal of the third NVM cell, and

wherein the controlling means further comprises:

means for coupling the fourth bit line to the first voltage source during the first phase; and

means for decoupling the fourth bit line from the ground source, and coupling the fourth bit line to the secondary signal source at the end of the first phase.

18. The memory circuit according to Claim 13, wherein the secondary signal source comprises a current source.

19. The memory circuit according to Claim 13, wherein the secondary signal source comprises a voltage source connected to a resistor.

20. The memory circuit according to Claim 13, wherein the secondary signal source comprises a third NVM cell.

21. A method for sensing a programmed/erased state of a selected non-volatile memory (NVM) cell within a memory array, the memory array including a first bit line connected to a first terminal of the selected NVM cell, a second bit line connected to a second terminal of the selected NVM cell, a second NVM cell having a first terminal connected to the second bit line, and a third bit line connected to a second terminal of the second NVM cell, the method comprising:

during a development phase:

coupling the first bit line to a voltage source,

coupling the second bit line to a sense amplifier,

coupling the third bit line to a force neighbor signal source, and

applying a gate voltage to the first and second NVM cells, whereby a current flows through the first NVM cell to generate a cell signal on the first terminal of the second NVM cell that develops at a first rate; and

during a read phase subsequent to the development phase, determining a programmed/erased state of the selected non-volatile memory cell by causing the sense amplifier to compare the cell voltage developed on the first bit line with a reference voltage,

wherein the forced neighbor signal source is selected such that a forced neighbor signal develops on the third bit line at a second rate similar to the first rate such that a voltage across the second NVM cell is minimized during the development phase.

22. The method according to Claim 21,

wherein the memory array also includes a reference cell having a first terminal connected to the voltage source and a second terminal connected to a second input terminal of the sense amplifier, and a third resistor connected between the second terminal of the reference cell and the ground source, and

wherein the method further comprises turning on the reference cell during the development phase such that a reference current is generated through the third resistor, thereby causing the reference voltage to develop on the second terminal of the sense amplifier.

23. The method according to Claim 21, further comprising, during the development phase:

coupling the second bit line to a first terminal of a first resistor, the first terminal of the first resistor also being connected to a first input terminal of the sense amplifier, wherein the first resistor includes a second terminal connected a ground source, and

coupling the third bit line to a first terminal of a second resistor, the first terminal of the second resistor also being connected to the forced neighbor signal source, wherein the second resistor includes a second terminal connected the ground source,

wherein the second resistor and the forced neighbor signal source are selected such that a forced neighbor current is generated on the third bit line that is equal to the reference current flowing through the third resistor.

24. The method according to Claim 21, further comprising, during the development phase:

coupling the second bit line to a first terminal of a first resistor, the first terminal of the first resistor also being connected to a first input terminal of the sense amplifier, wherein the first resistor includes a second terminal connected a ground source, and

coupling the third bit line to a first terminal of a second resistor, the first terminal of the second resistor also being connected to the forced neighbor signal source, wherein the second resistor includes a second terminal connected the ground source,

wherein the second resistor and the forced neighbor signal source are selected such that, when the threshold voltage of the selected NVM cell equals the threshold voltage of the reference cell, the drain-to-source voltage across the neighbor cell is zero.